

WELCOME  
WELCOME

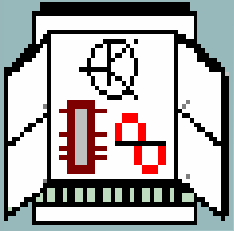
to

Slideshow presentation  
Slideshow presentation

of

ECAD package  
ECAD package

OPUSER XP  
OPUSER XP

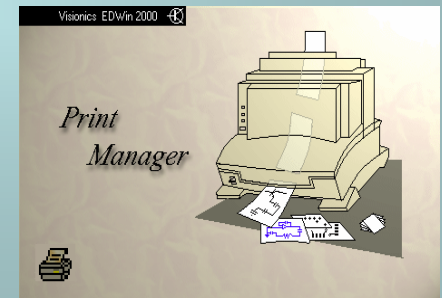
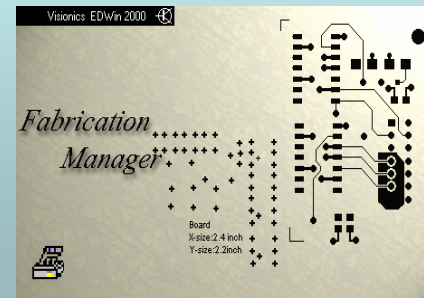
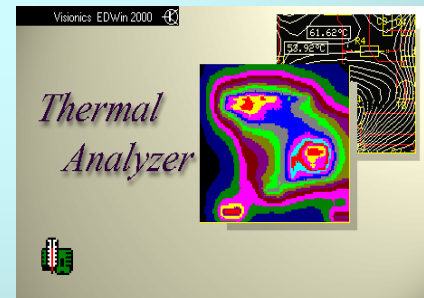
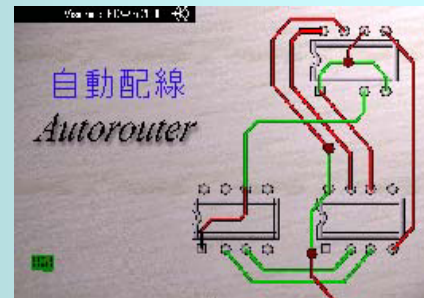
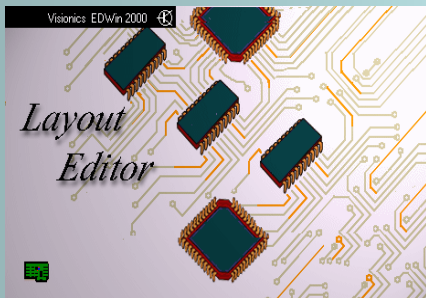
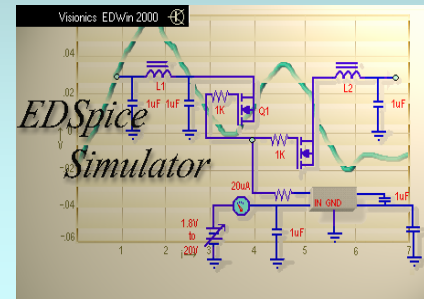
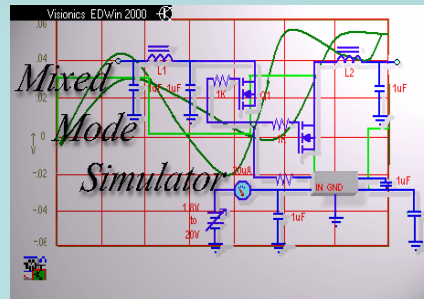
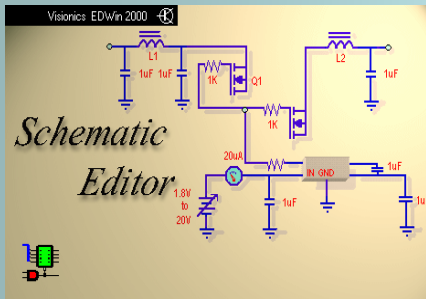


# *What is OPUSER XP ?*

*OPUSER XP is a state-of-the-art CAD/ CAE software package. It provides an electronic engineer with sophisticated tools to capture an electronic circuit in the form of schematic diagram and/ or PCB layout.*

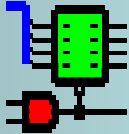
# Totally integrated project database

**OPUSER XP**

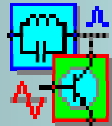


# *OPUSER XP Family*

## Individual Project Modules



Schematic Editor



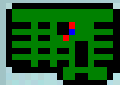
Mixed Mode Simulator



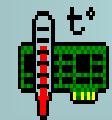
EDSpice Simulator



VHDL Compiler



PCB Layout Editor

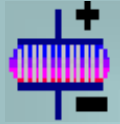


Thermal Analyser



3D Viewer

# *OPUSER XP Family*



Electro Magnetic Analyser



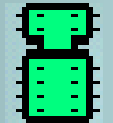
Fabrication Manager



Library Explorer



Library Browser



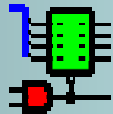
Part Editor



List of Materials Editor



Conversion Manager



Symbol Library Editor



Model Parameter Library Editor

# OPUSER XP Family

3 packages Basic, Plus, Plus+

## Basic package



Schematic Editor, Mixed Mode Simulator, PCB Layout Editor, Auto Router, Fabrication Manager, Library Explorer, Library Browser, Part Editor, List of Materials Editor, Conversion Manager, Symbol Library Editor, Model Parameter Library Editor

## Plus package



Schematic Editor, Mixed Mode Simulator, EDSpice Simulator, VHDL Compiler, PCB Layout Editor, Auto Router, Thermal Analyser, Fabrication Manager, Library Explorer, Library Browser, Part Editor, List of Materials Editor, Conversion Manager, Symbol Library Editor, Model Parameter Library Editor

## Plus+ package



Schematic Editor, Mixed Mode Simulator, EDSpice Simulator, VHDL Compiler, PCB Layout Editor, Auto Router, Thermal Analyser, Electro Magnetic Analyser, Signal Integrity Analyser, 3D Viewer, California Placer, Fabrication Manager, Library Explorer, Library Browser, Part Editor, List of Materials Editor, Conversion Manager, Symbol Library Editor, Model Parameter Library Editor,



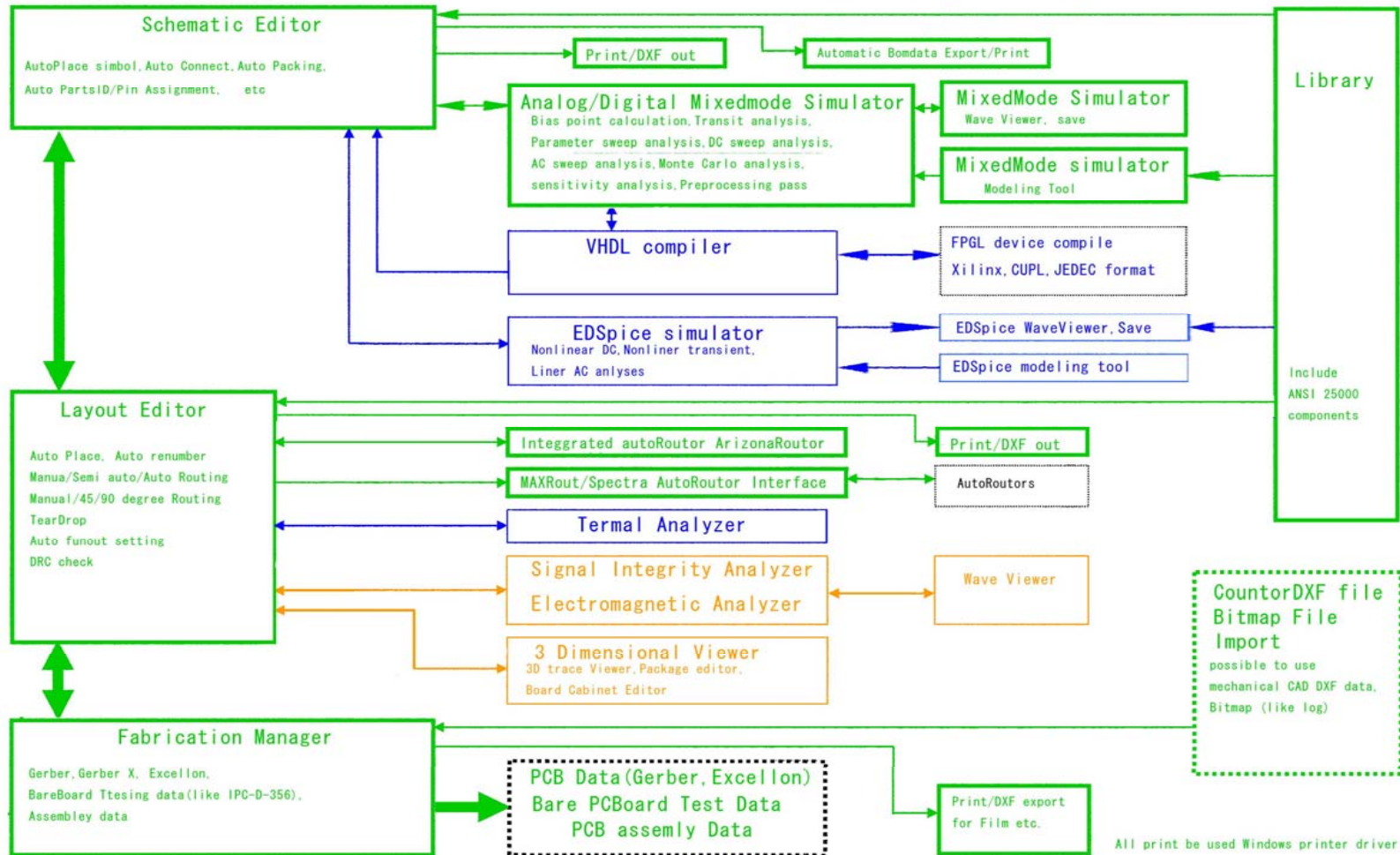
# OPUSER XP Family

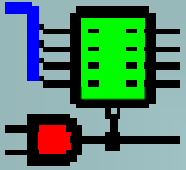
## OPUSER XP overview

Basic Package

Plus Package the expansion of a Basic Pack.

Plus+ Package the expansion of a Plus Pack.



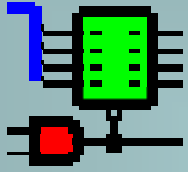


# *Schematic Editor*

## **Features**

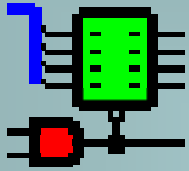
- ◆ Upto 99 Schematic sheets, 4m x 4m sheet size.
- ◆ Repeat, Rotate, Mirror and scale components with different colors.
- ◆ Real-time dragging of components and wires.
- ◆ Automatic package and pin assignment.
- ◆ Orthogonal and free mode manual routing.
- ◆ Automatic bus annotation.
- ◆ Block save, load, move and delete can be activated using shift key.
- ◆ Direct access to Mixed Mode & EDSpice simulation.
- ◆ Autorouting of connections.





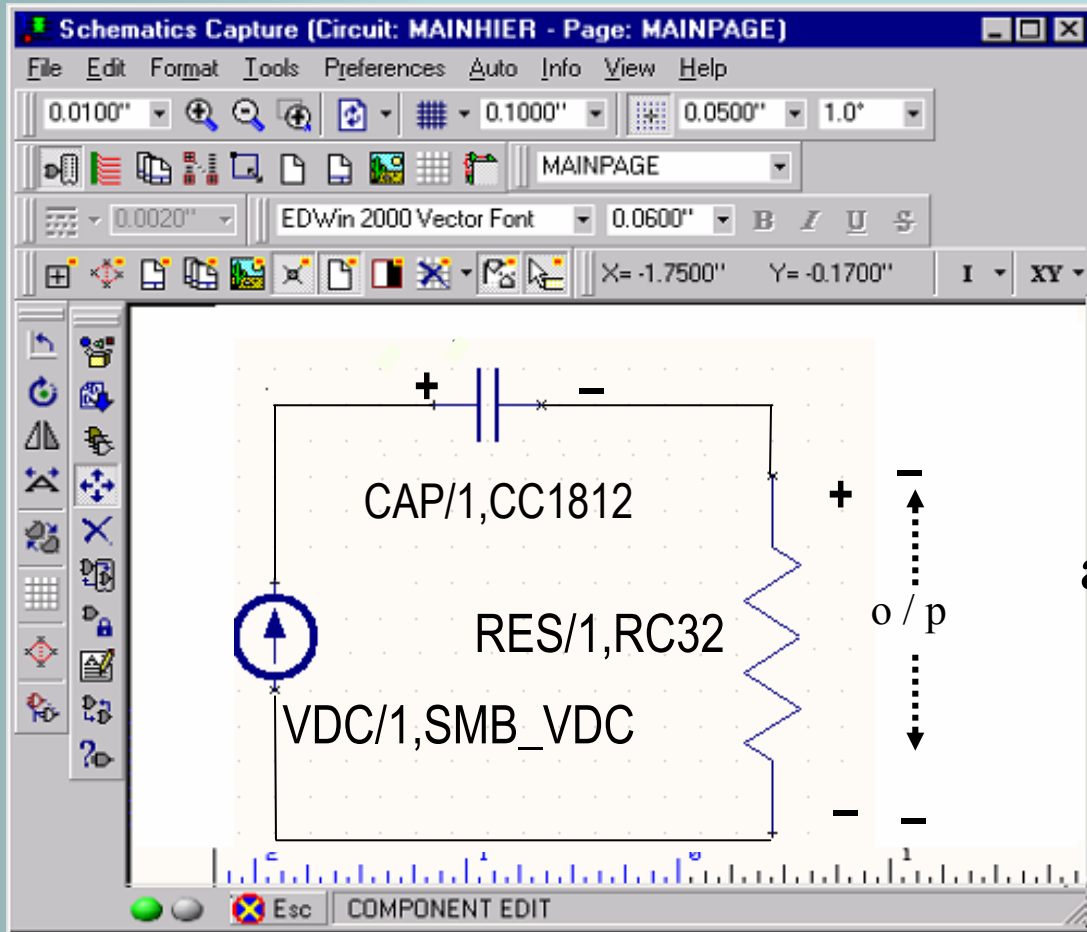
# *Schematic Editor*

- # Merging and splitting of nets possibility.
- # Swapping of component position.
- # Automatic component renumbering by swapping.
- # Component move by name, grid.
- # 4 different grid types for autoplacement.
- # Autorouting of wires with users preferences.
- # True type font (TTF) supported

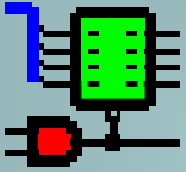


# Schematic Editor

## Logical Representation

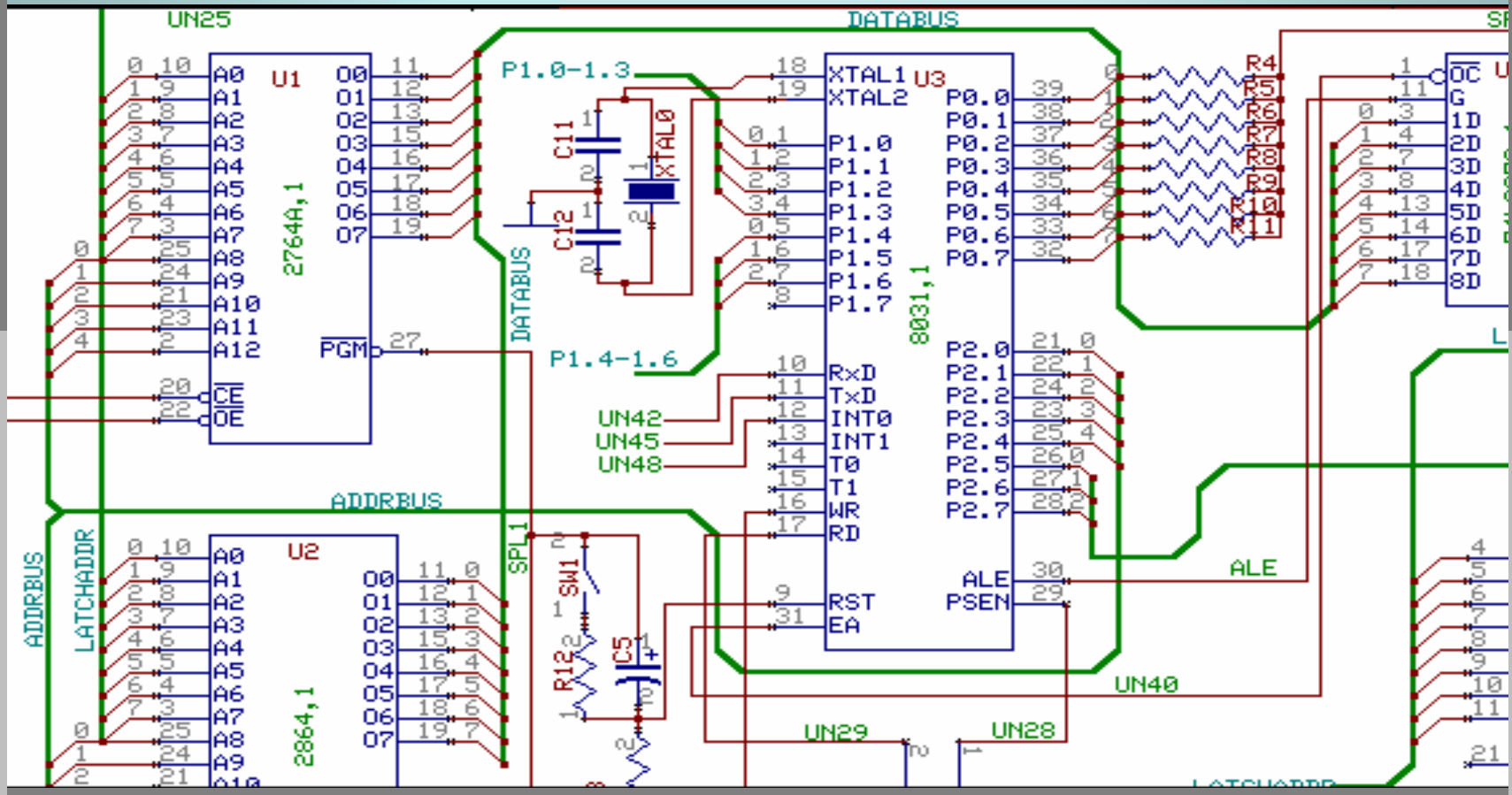


Multiple hierarchical levels  
with multiple  
pages within hierarchy.  
\* Full set of manual and  
automatic editing functions  
including autorouting and  
autoplacement



# Schematic Editor

*Elementary stage in circuit design.*



# *PCB Layout Editor*

## **Features**

- ⌘ 32 layers ( 28 route layers, 2 silk-screen layers, (front and back), 2 solder mask layers (front and back))
- ⌘ User definable trace sizes & pad sizes.
- ⌘ Curved traces with user specified radius
- ⌘ 1 micron grid resolution-Fine grid 10 micron
- ⌘ SMT, fine-line support
- ⌘ Component repeat, rotate and mirror.
- ⌘ Component move by name, grid
- ⌘ Component, gate and pin swap.
- ⌘ Component auto renumbering

# *PCB Layout Editor*

## **Features**

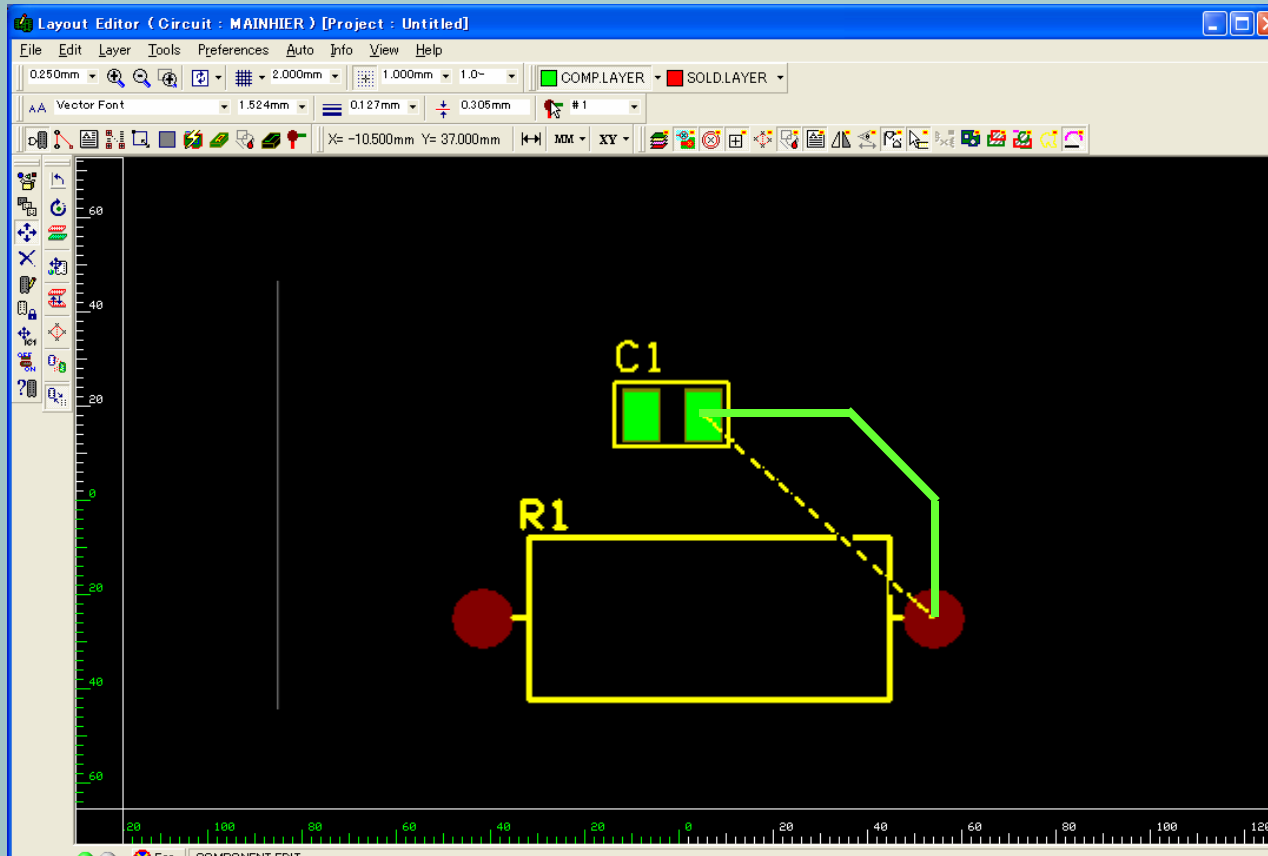
- ↔ Autoplacement of component
- ↔ 8 different grid types of autoplacement.
- ↔ Direct access to Standard and Arizona autorouters.
- ↔ Automatic component renaming.
- ↔ Trace pattern repeat
- ↔ On-line, multi-layer routing with automatic via insertion.
- ↔ Buried and unburied via supported

# *PCB Layout Editor*

- ⇔ Pin-to-pin, free or 45° routing
- ⇔ Change segment side and width, trace side and width.
- ⇔ Copper Planes and Copper Pour Areas may be created with user definable cross-hatch or solid fill.
- ⇔ Design Rule check
- ⇔ Net connectivity check
- ⇔ Display of single net supported



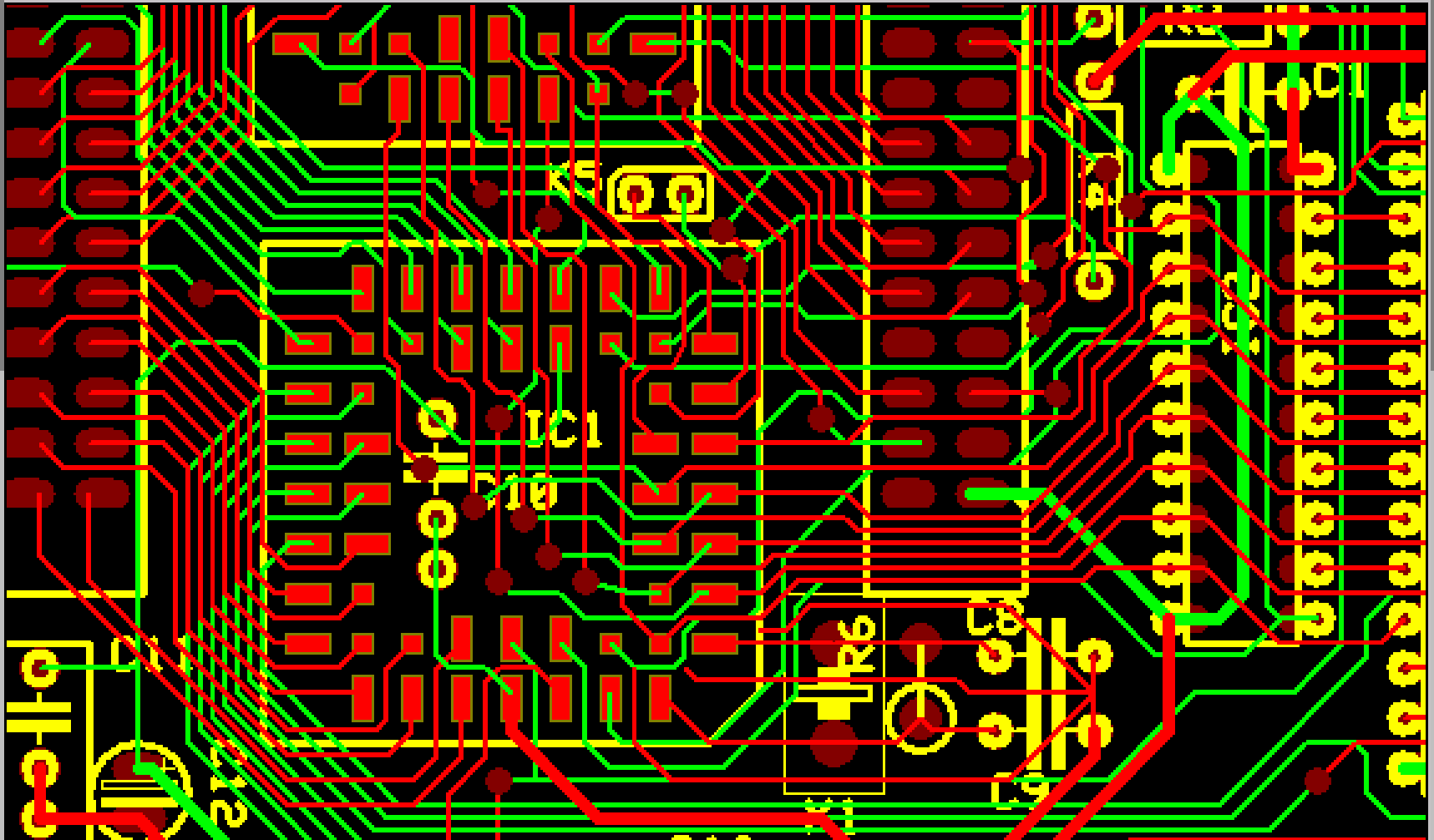
# PCB Layout Editor



*Provides comprehensive and auto-interactive design environment based on rule driven grid free architecture.*

# *PCB Layout Editor*

*Alternative starting point of PCB design process*





# *Arizona Autorouter*

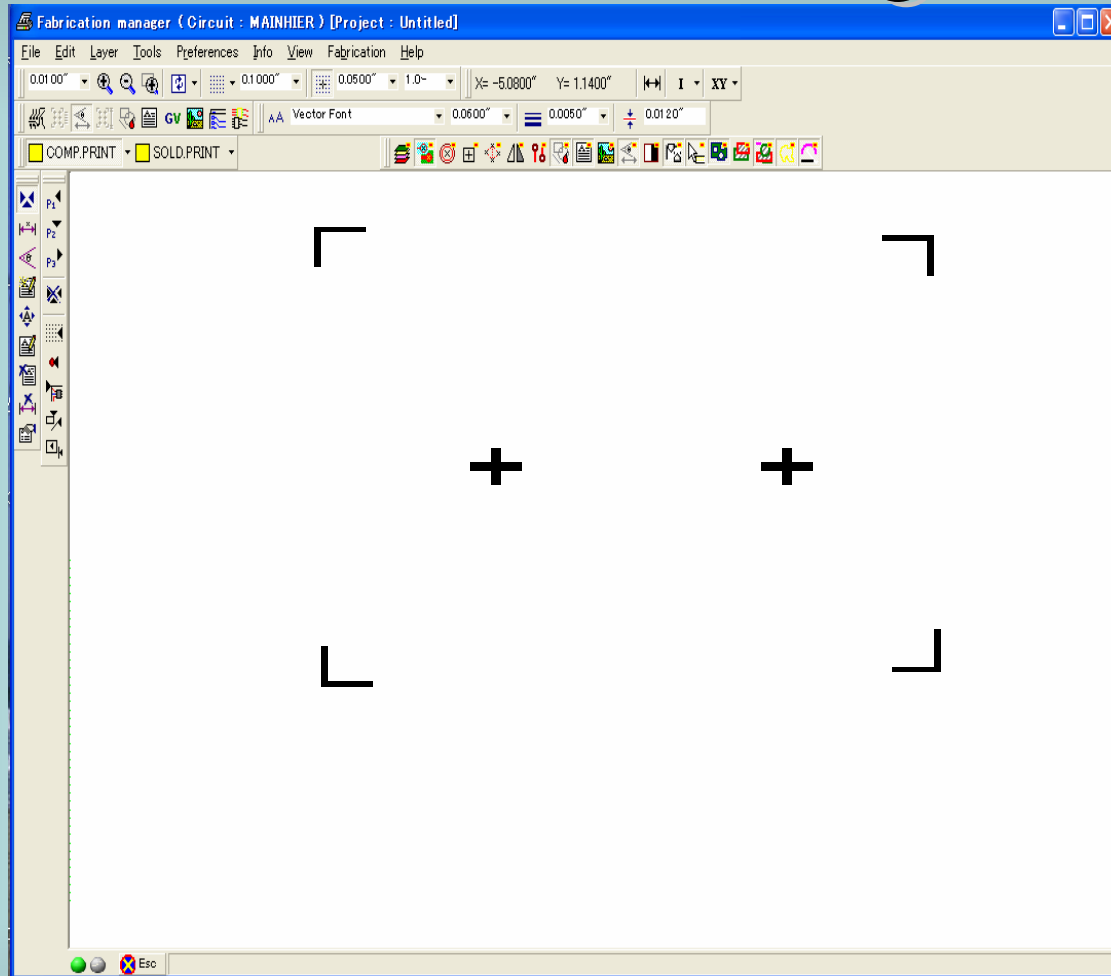
## **Features**

- ❖ **OPUSER XP's** own integrated Autorouter
- ❖ Fully Automated and Interactive Modes
- ❖ Routing by Strategies or Preset Parameters
- ❖ User Definable strategies
- ❖ Single, Double and Multi Layer Routing possible
- ❖ Grid less routing

# *Fabrication Manager*

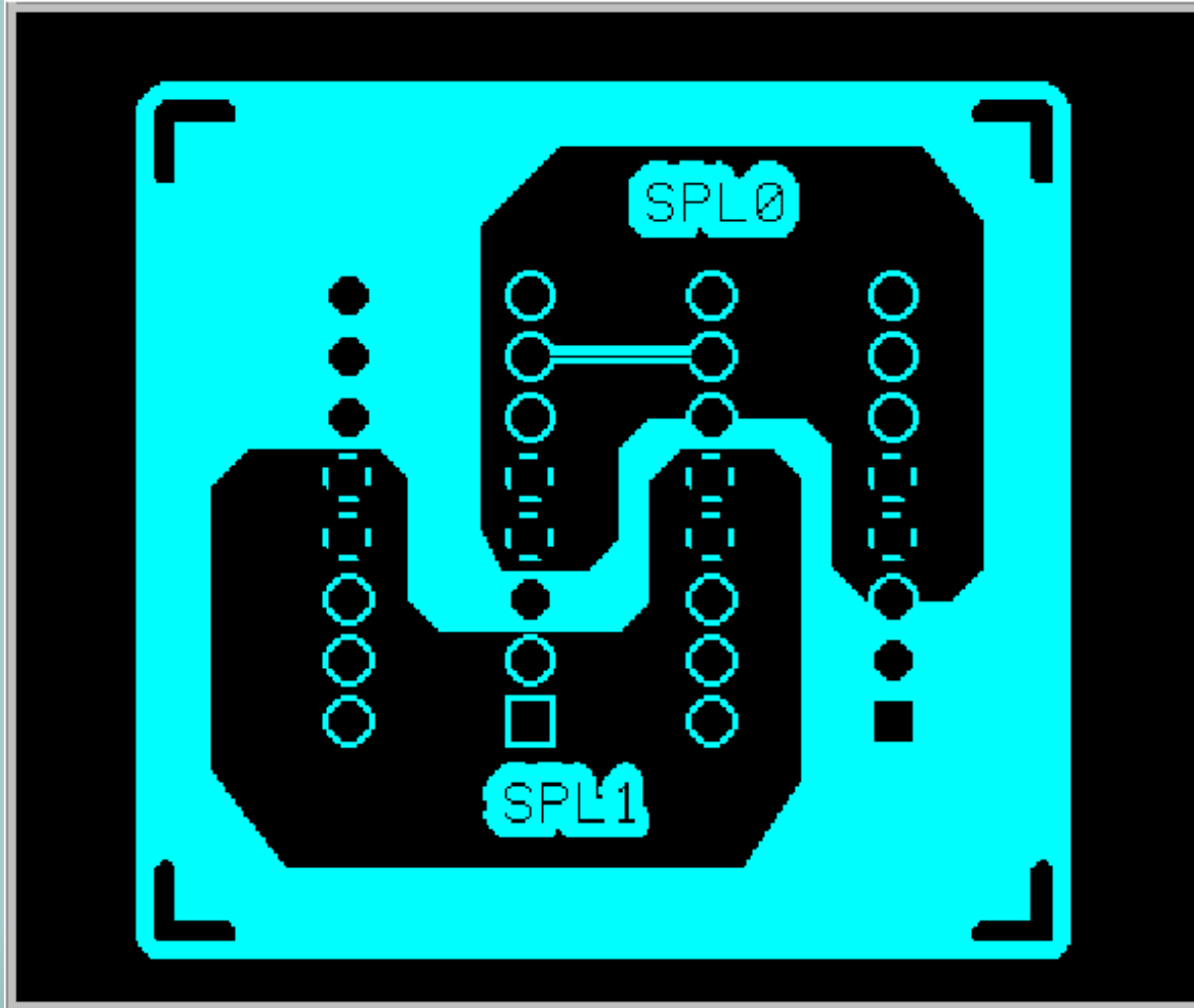
- ✔ Final stage in the PCB design process
- ✔ Creation of Copper Planes and Copper Pour Area supported
- ✔ Converts the Design Data (Layout) into manufacturing / documentation outputs such as:
  - \* Dimension Drawings
  - \* Layer Artworks
  - \* NC-Drill Template
  - \* Gerber for Printer / Plotter
  - \* Generic Pick & Place.
- ✔ Superimposing of artworks supported
- ✔ Connectivity check for artwork supported
- ✔ Negative plot for artwork supported

# *Fabrication Manager*



*All functions needed for generating PCB manufacturing documentation GERBER and NC-Drill outputs*

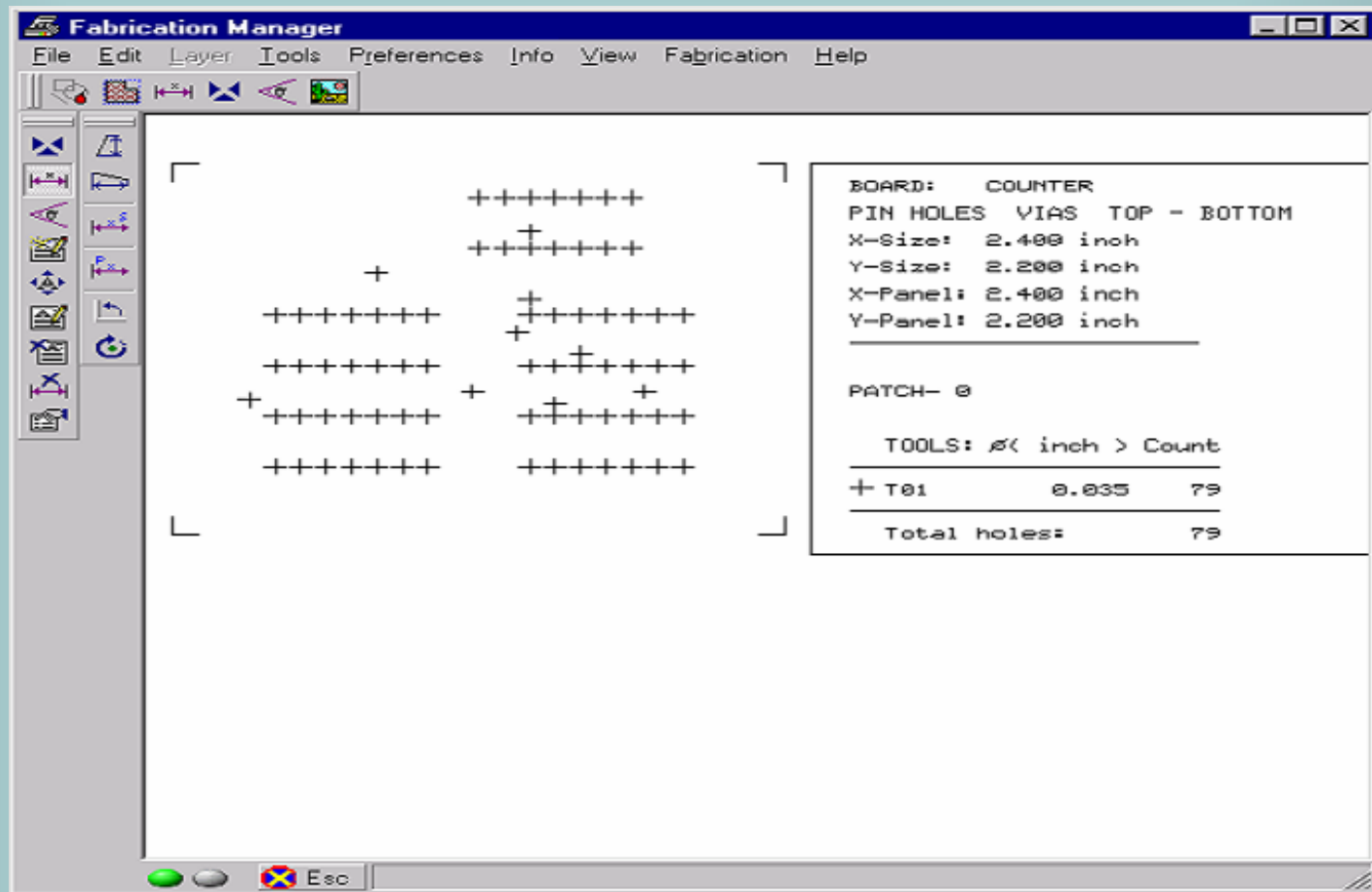
# *Copper Pour Area*



*Allows assigning one or more Copper Pour Areas on a layer.*

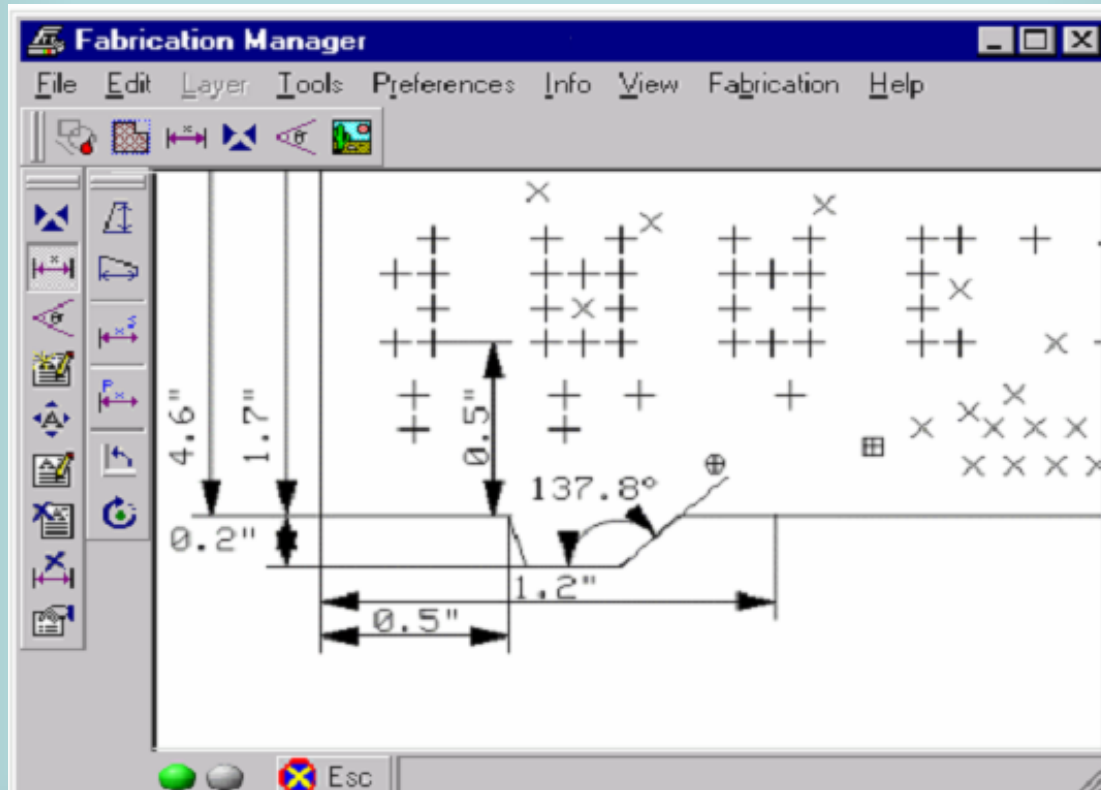


# NC-Drill Template



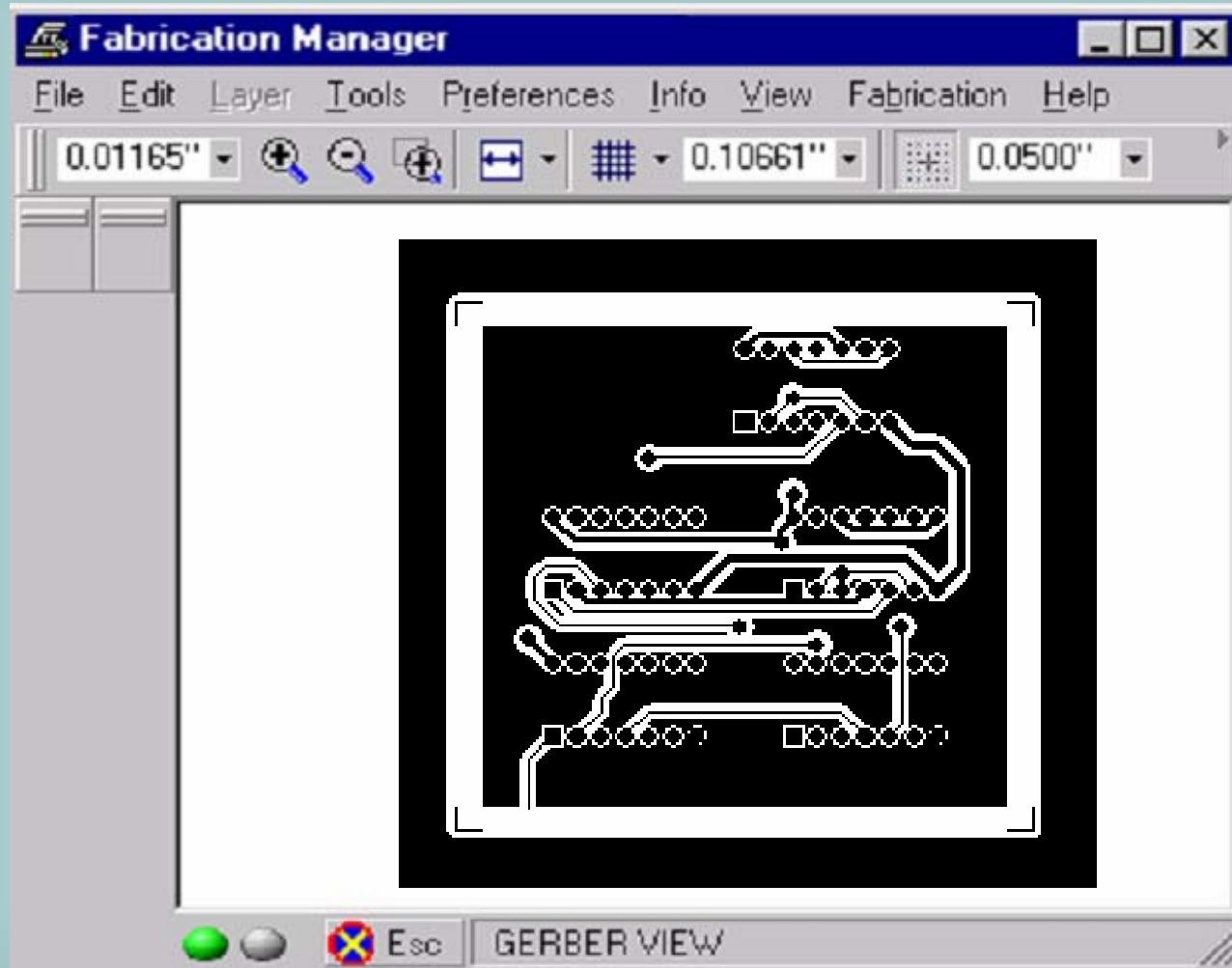
*NC Drill file containing tool selection command and hole coordinates for automatic drilling of component pins and via holes.*

# *Dimension Drawing*

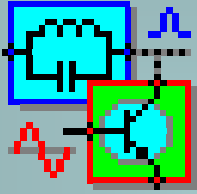


*Facilitates linear and angular dimensioning of components, pads and board outlines*

# *Artwork in Gerber format*



Superimposing of artworks



# *Simulation*

## *Features*

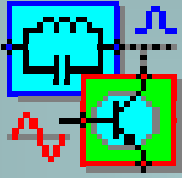
Simulators Provided by **OPUSER XP**

### Circuit level

- ✘ Mixed Mode Simulator
- ✘ EDSpice Simulator (Mixed Mode)

### Board level

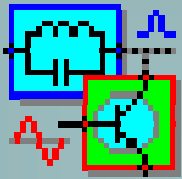
- ✘ Thermal Analyzer
- ✘ Electromagnetic Analyzer
- ✘ 3D Viewer



# *Mixed Mode Simulator*

## *Features*

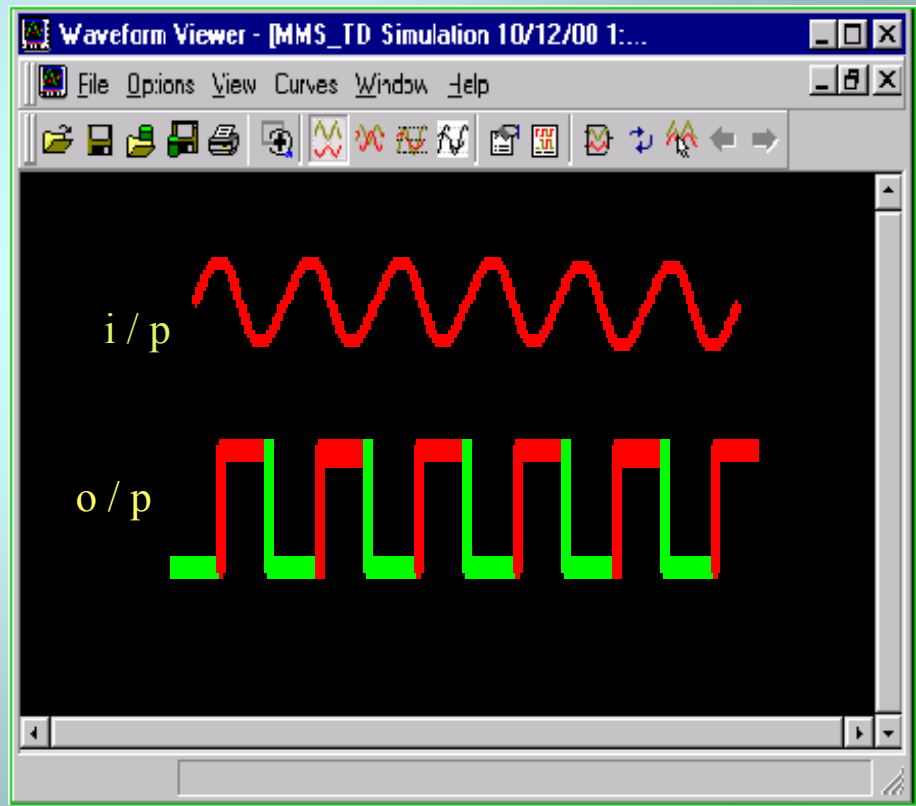
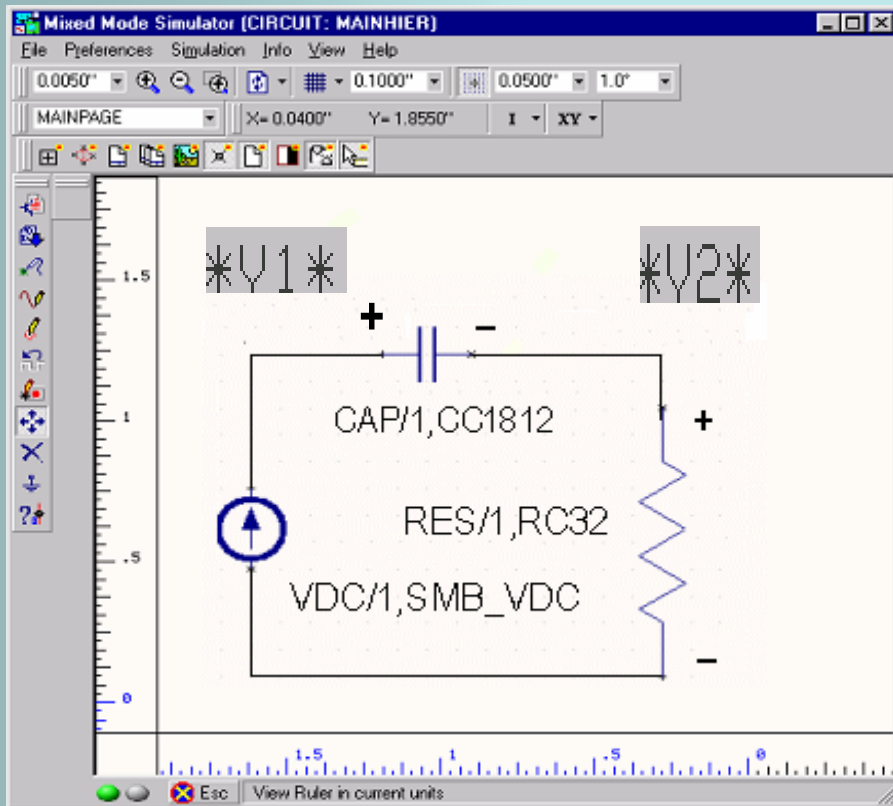
- Mixed Mode Simulator
  - \* Simulation for hierarchical circuit is supported
  - \* Matrix solving error can be automatically fixed
  
- Temperature can be set on individual circuits.
  
- Graphical output through Waveform Viewer on screen.
  
- Waveform can be created as a symbol and may be placed wherever required in capture



# Mixed Mode Simulation

*OPUSER XP Simulator*

*Waveform Viewer*





# *Mixed Mode Simulation*

## Types of analysis

- Bias Point Calculation
- Transient Analysis
- Parameter Analysis
- Fourier Analysis
- DC Sweep Analysis
- AC Sweep Analysis
- Monte Carlo Analysis
- Sensitivity Analysis

# *EDSpice Simulator*

## *Features*

- ⇒ Temperature can be set on individual circuits.
- ⇒ Improved convergence algorithms (Gmin / Source stepping).
- ⇒ Circuit size is only limited by memory.
- ⇒ Supports Code models and user-defined nodes.
- ⇒ Subcircuits can be imported to **OPUSER XP** supplied by manufactures

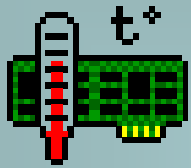


# *EDSpice Simulator*

## *Features*

Analyses that may be done:

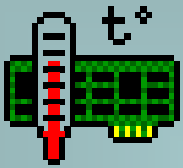
- γ Small Signal AC Analysis
- γ DC Transfer Function Analysis
- γ Distortion Analysis
- γ Noise Analysis
- γ Operating Point Analysis
- γ Pole-Zero Analysis
- γ DC/ AC Sensitivity Analysis
- γ Transfer Function Analysis
- γ Fourier Analysis



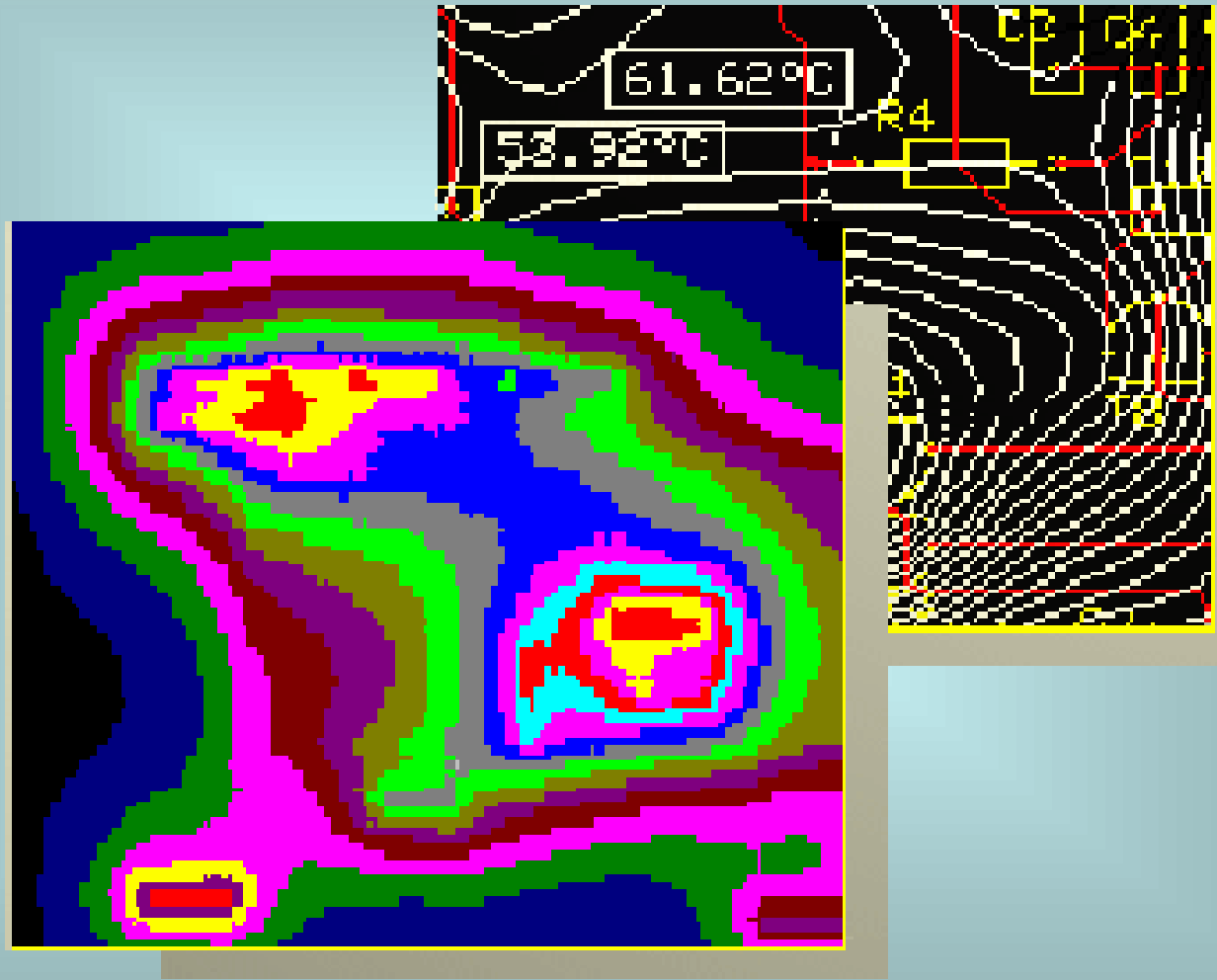
# *Thermal Analyzer*

## *Features*

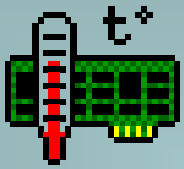
- ❏ Plug-in-tool for **OPUSER XP**
- ❏ Enables you to perform comprehensive thermal analysis of your PCB designs.
- ❏ Thermal parameters are attached to parts
- ❏ Analysis using component thermal parameters set from external library or User Defined, board parameters and environmental parameters such as cooling.
- ❏ Highlights hotspots in the board.
- ❏ Results displayed using Isotherms and Color mapping scheme.



# *Thermal Analyzer*

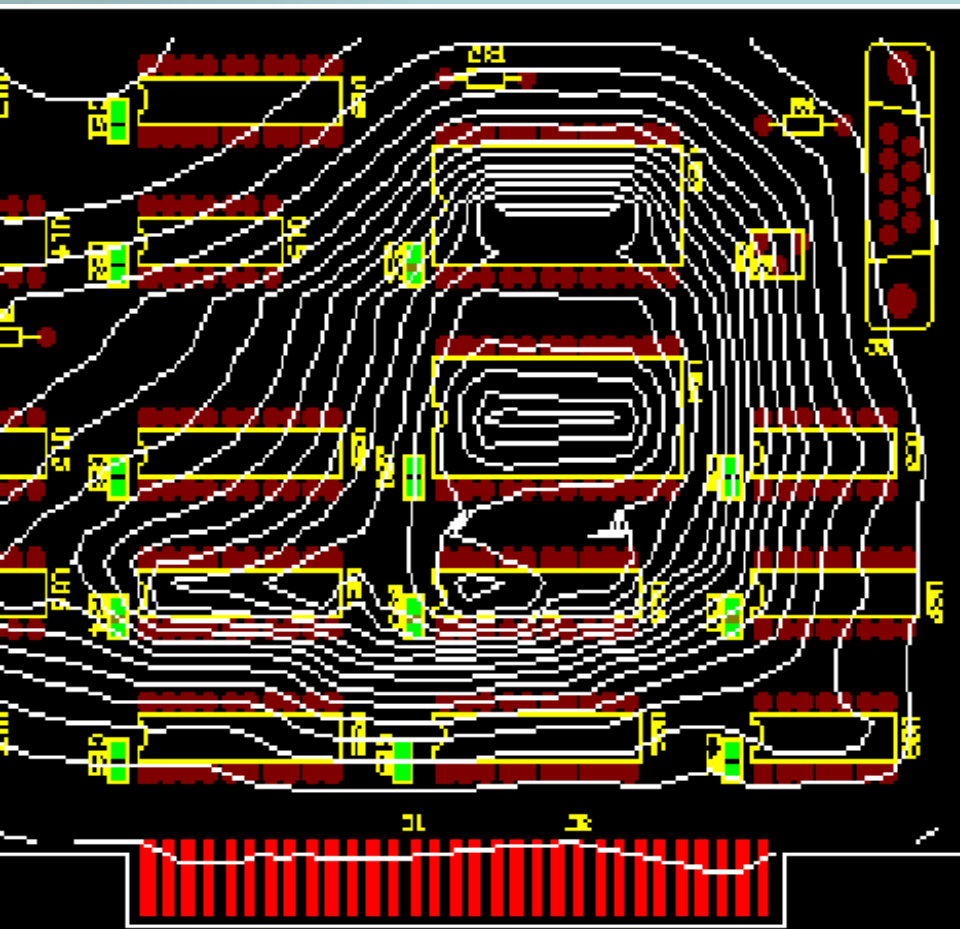


*Highlights possible hotspots on the board*

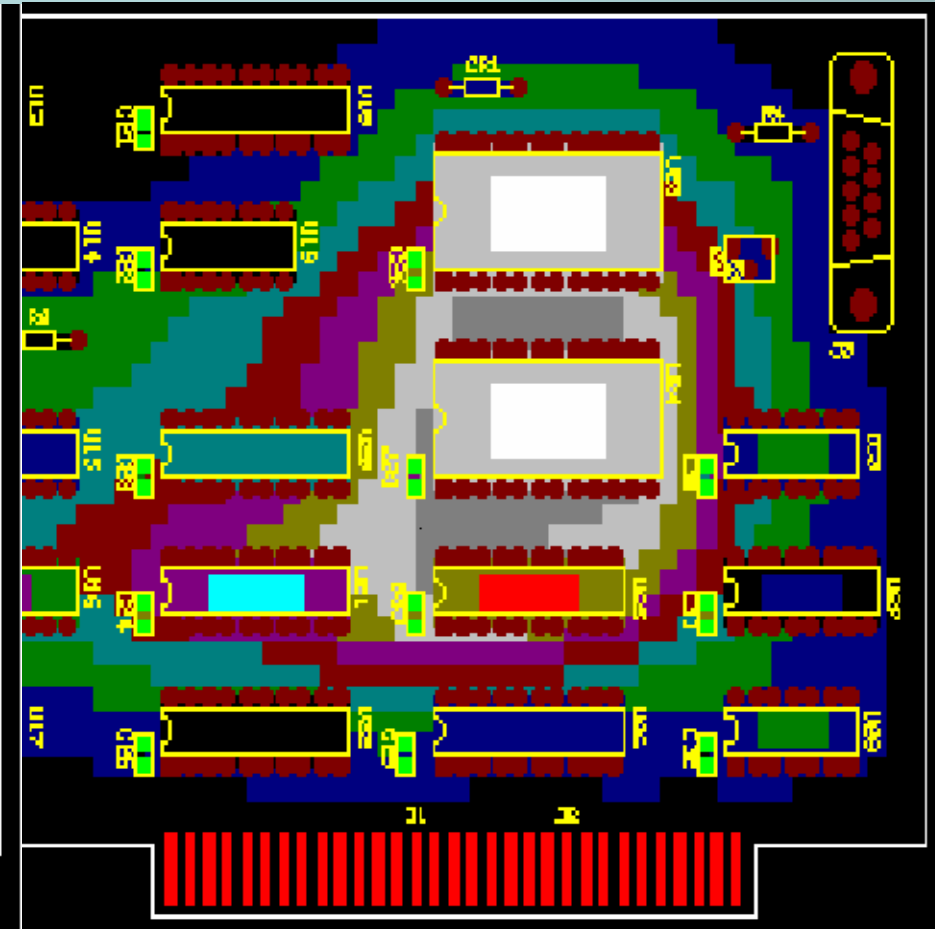


# *Thermal Analyzer*

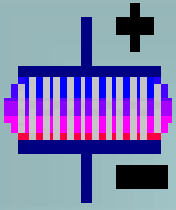
*Isotherm Display*



*Colored Map*



*Results displayed through Isotherms and Colored Map*



# *Electromagnetic Analyzer*

## **Plug-in-tool for OPUSER XP**

Tool to calculate and measure the magnetic interface of the PCB design

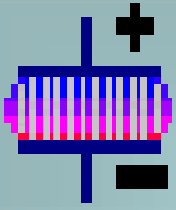
Finite Difference Time Domain based Electromagnetic Field solver and simulator.

All to help to comply with the EMC rules for CE certification and to maintain a proper documentation. Highlights hotspots in the board.

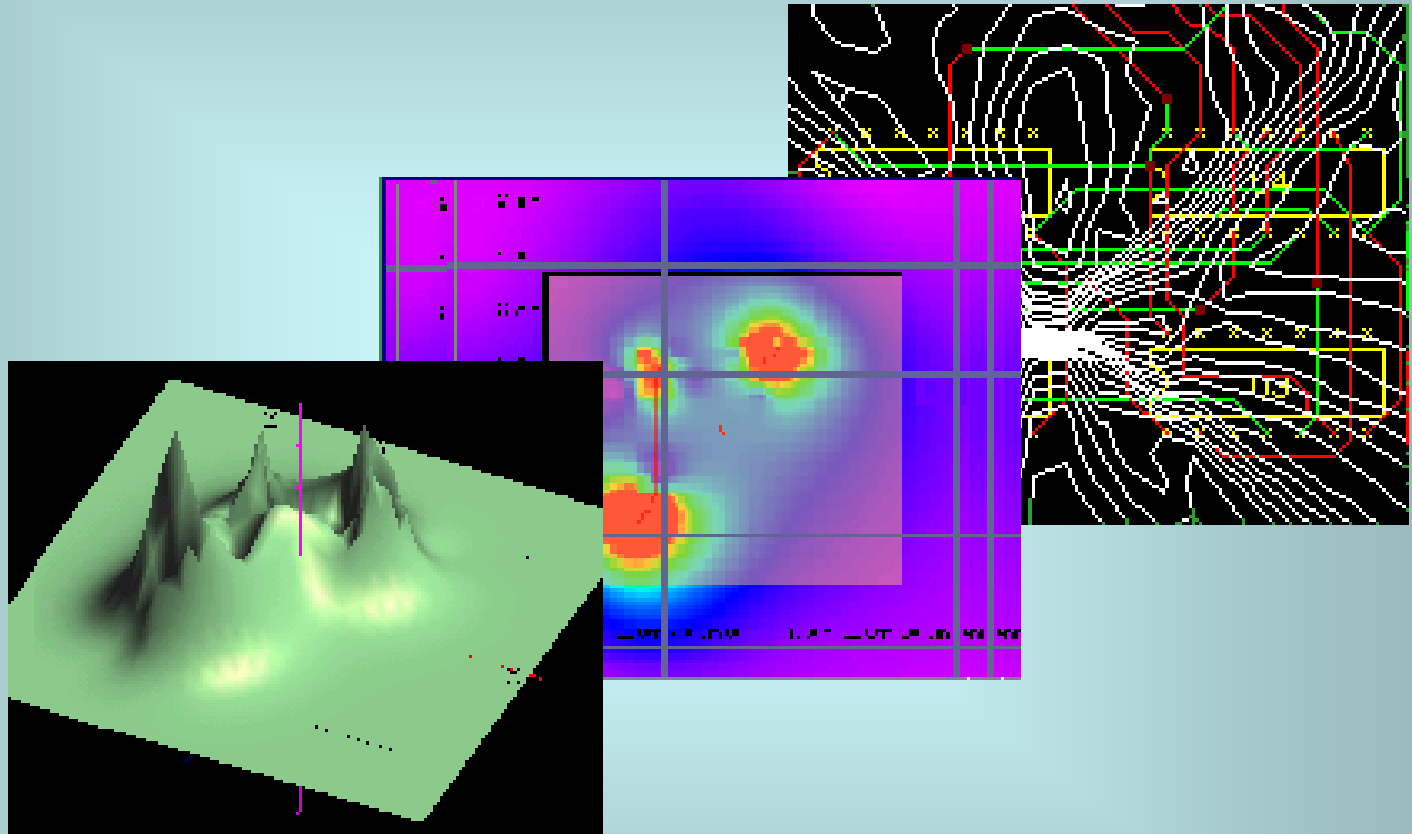
Results displayed using Isolines and color Mapping scheme.

Special add-on option "Signal Integrity Simulation".

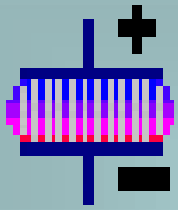




# *Electromagnetic Analyzer*



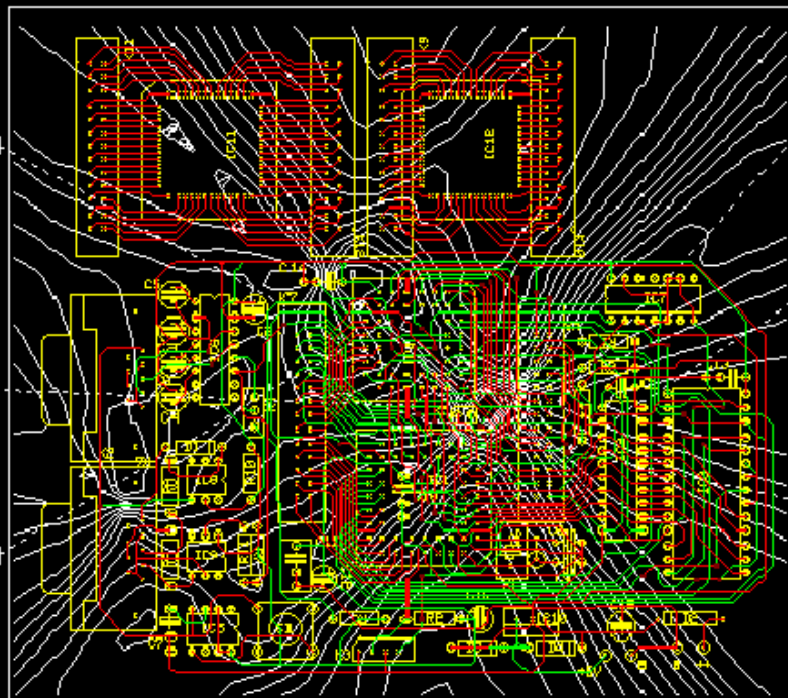
*Find out the cross talks, improper placement, shielding and more where your design is still a diagram*



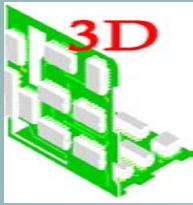
# Electromagnetic Analyzer

*Isolines*

*Colored Map*



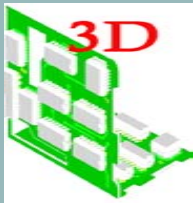
*Results displayed through Isolines and Colored Map*



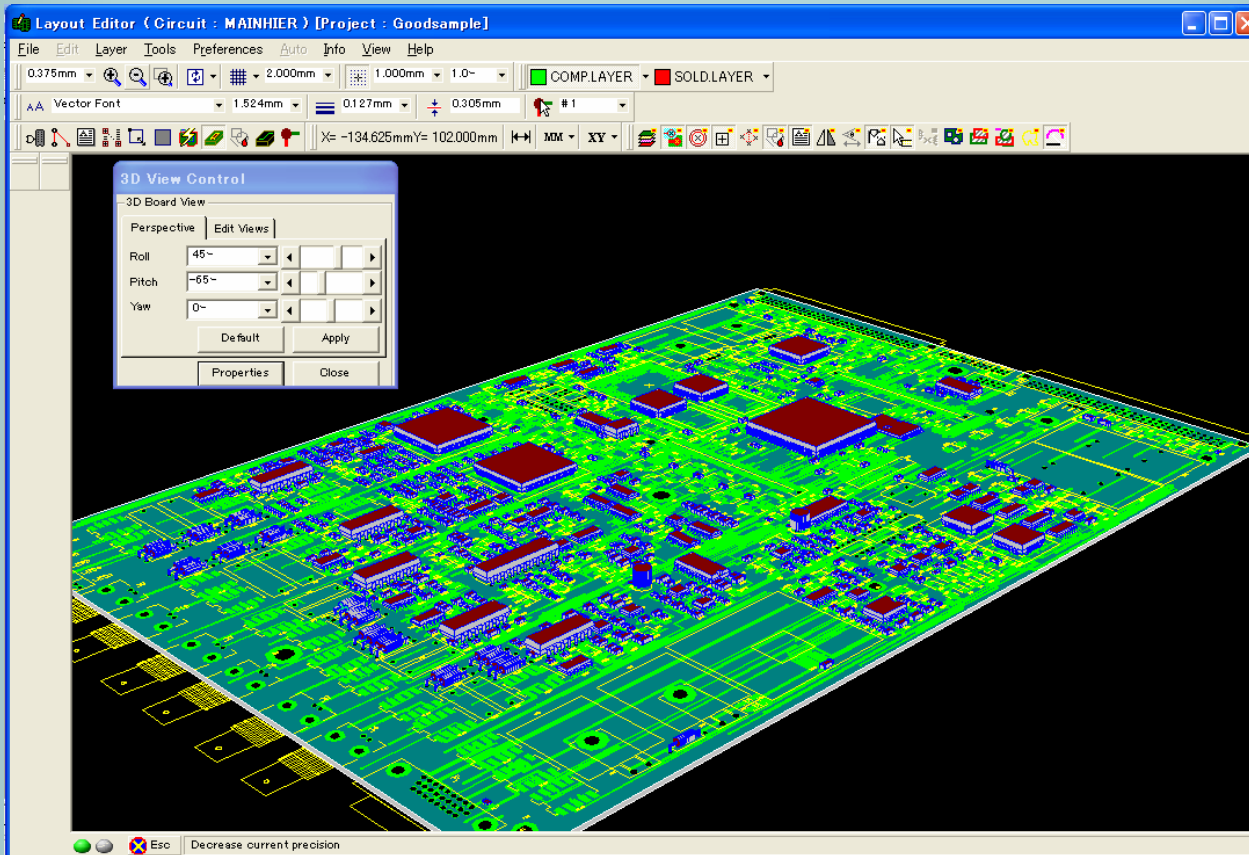
# *3D Viewer*

## *Features*

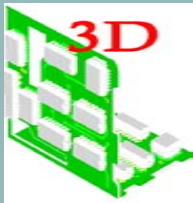
- ❏ Plug-in-tool for **OPUSER XP**
- ❏ Enables you to check components assembled PCB of your PCB designs.
- ❏ Enables you to check via for multilayer board of your PCB designs.
- ❏ Possible to check from any angle (X 360 Y360 Z360).
- ❏ Size parameters are attached to parts



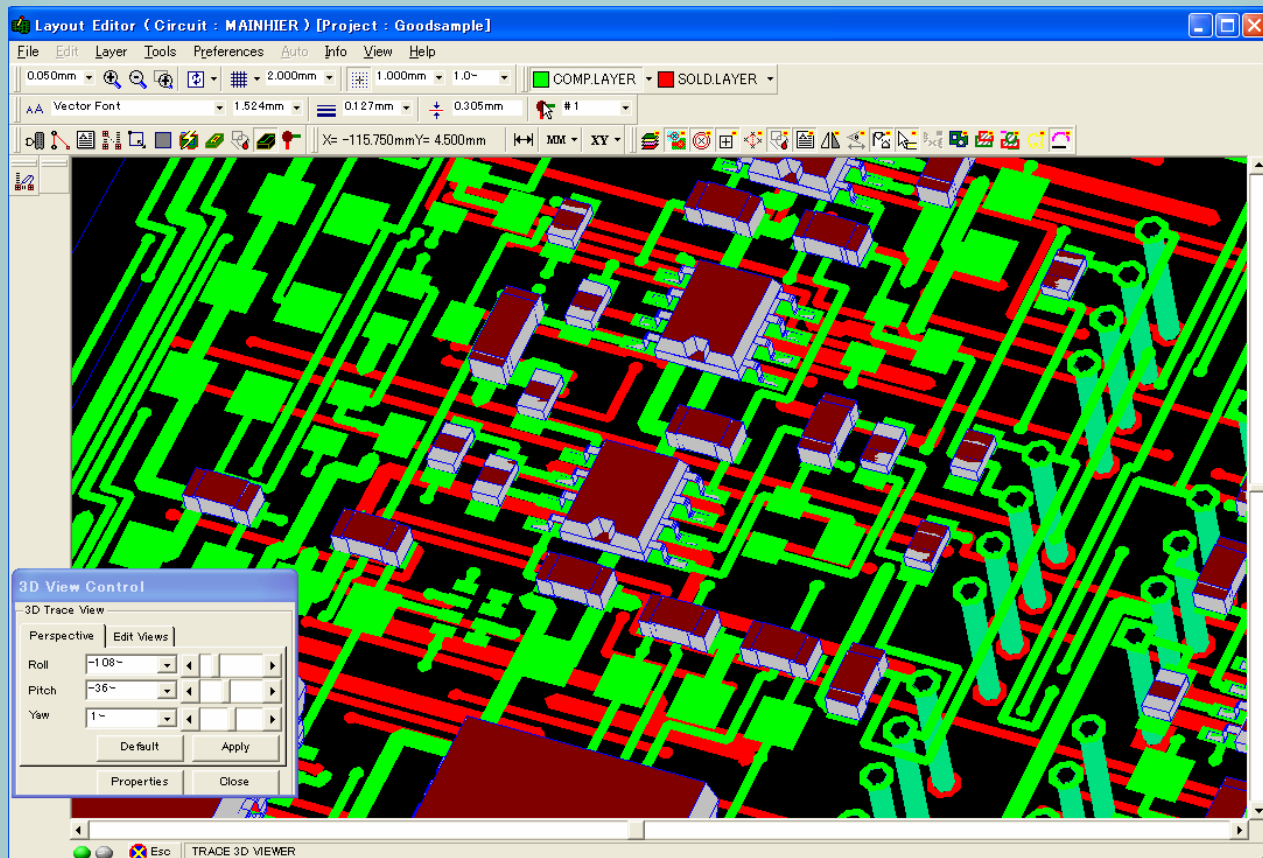
# 3D Viewer



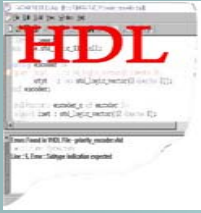
*3D Board Viewer*



# 3D Viewer



*3D Trace Viewer*



# *VHDL Compiler*

## *Features*

- Compiles the source file and generates **wirelist** output file.
- Possible to import output file directly into OPUSER XP.
- Generates simulatable models in Mixed Mode &  
EDSpice Model Generators
- Converts the (\*.wrs) file to **Xilinx**, **CUPL** & **JEDEC** formats.



# VHDL Compiler

The screenshot shows the VHDL Editor window with the following content:

```
library ieee;
use ieee.std_logic_1164.all;

entity serial_in_serial_out_shift_register is
port (
    clk : in std_logic;
    ce   : in std_logic;
    inet : in std_logic_vector(0 to 7);
    oout : out std_logic_vector(0 to 7);
end entity;

architecture sinsoutshift_a of serial_in_serial_out_shift_register is
    signal inet : std_logic_vector(0 to 7);
begin
    process (clk, ce)
    begin
        if ce = '1' then
            if (clk = '1') and (clk'event) then
                inet(7) <= inet(6);
                inet(6) <= inet(5);
                inet(5) <= inet(4);
                inet(4) <= inet(3);
                inet(3) <= inet(2);
                inet(2) <= inet(1);
                inet(1) <= inet(0);
            end if;
        end if;
    end process;
end architecture;
```

The compile menu is open, showing the following options:

- Compile (F7)
- Compile & Import to Opuser (Ctrl+F7)
- Create MM Model (Ctrl+F8)
- Create EDSpice Model (Ctrl+F9)
- Create XILINX Output (Ctrl+F10)
- Create CUPL Output (Ctrl+F11)
- Create JEDEC Output (Ctrl+F12)

The output window at the bottom shows the message: "Compiled with no errors; Generated : C:\%OPUSER%\JOB%SERIAL\_IN\_SERIAL\_OUT\_SHIFT\_REGISTER.wrs"

All keywords present in the source are highlighted in Blue.

On double clicking the error the corresponding line in the editor window will get highlighted in Red.

# *Library Modules*

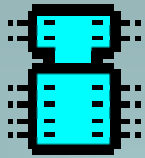
✉ *Part Editor*

✉ *Padstack Editor*

✉ *Library Explorer*

✉ *Library Browser*





# Library Explorer

**Library Explorer : ( C:\%OPUSER%LIB )**

Library Editor (Editing Part : C:\%OPUSER%LIB\74CMOS.PART\74AG00)

File Edit View Help

Part Details	
<b>General</b>	
Name	74AG00
Prefix	U
Description	@quad 2-IP +ve NAND
Manufacturer	Generic
Technology	ACMOS
Type	Digital,Gate,NAND
External Index Code	
Part Source Library	C:\%OPUSER%LIB\74CMOS.PART
<b>Package Details</b>	
Package	DIP14/300
Package Type	PMD,DIP,DIP Narrow
Package JEDEC Name	
Package Source Library	C:\%OPUSER%LIB\PMD.PACKAGE
<b>Simulation Parameters</b>	
<b>Thermal Parameters</b>	

Constituent Groups	
<b>(1) Group : 1 (2NAND) No UnAssigned</b>	
Group Name	1
Symbol	2NAND
Un-Assigned Entries	0
MM Simulation Function	505
EDSpice Element Code	A
EDSpice Model Code / SubCircuit	D_NAND
EDSpice Variant / Library	2NAND
Symbol Library	C:\%OPUSER%LIB\A.DGTAL.SYMBOL
<b>(2) Group : 2 (2NAND) No UnAssigned</b>	
<b>(3) Group : 3 (2NAND) No UnAssigned</b>	
<b>(4) Group : 4 (2NAND) No UnAssigned</b>	

Package : DIP14/300

COMPNAME  
COMPDESC

(1) Group : 1 (2NAND)

PA PA COMPNAME PA  
X(B) X X(3)

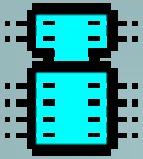
COMPDESC

View Symbol  
View Package  
**Edit Part**  
Send To  
Cut Ctrl+X  
Copy Ctrl+C  
Paste Ctrl+V  
Delete Shift+Del  
Rename  
Select All Ctrl+A

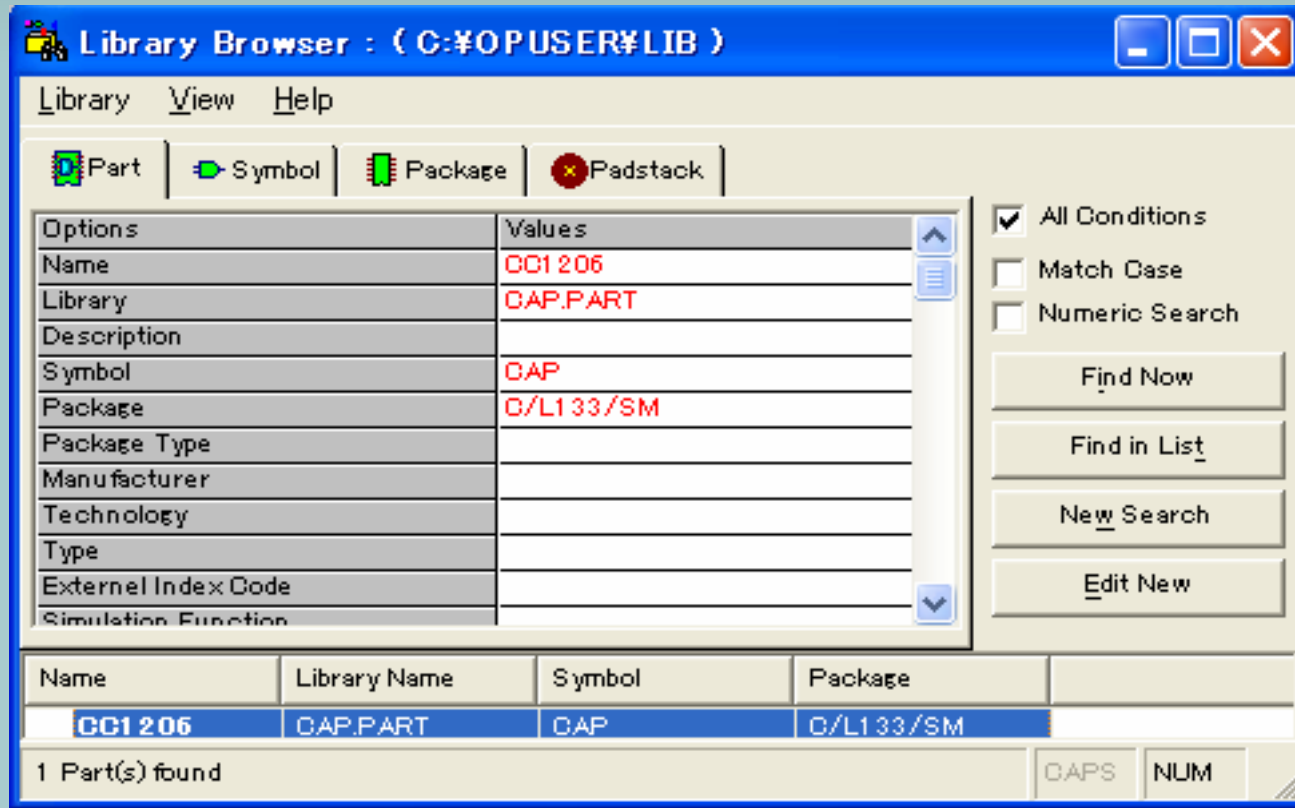
All

Part Edit Symbol Package Padstack Board Cabinet

*Easy to use like Windows Explorer with standard Windows editing features like Cut, Copy, Paste, Send to, Drag Drop and Select all.*



# Library Browser



*Object oriented user defined search for library elements (Parts/ Symbols/ Packages/ Padstack) from the libraries. Browser appends to the search list according to user preference.*

**DISTRIBUTOR**



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